SLR-VS – 1

Seat No.	

M.Sc. (Part – I) (Semester – I) Examination, 2014
ELECTRONICS (CGPA Pattern)
Paper – I : Mathematical Techniques

Day and Date : Monday, 21-4-2014 Total Marks : 70
Time : 11.00 a.m. to 2.00 p.m.

Instructions *: 1) Attempt **five** questions.*
*2) Question **1** and **2** are **compulsory**.*
*3) Attempt **any three** from Q. **3** to Q. **7**.*
*4) Figures to the **right** indicate **full** marks.*

1. A) Select correct alternatives : **8**

1) By Laplace transformation the time domain function reduces to _____ domain.
   a) Time b) Frequency
   c) Phase d) All of these

2) Laplace transformation of $\sin \omega t$ = _____
   a) $\frac{s}{s^2+\omega^2}$ b) $\frac{\omega}{s^2+\omega^2}$ c) $\frac{s}{\omega}$ d) $\frac{\omega}{s}$

3) A matrix for which aij = 0 for $i \neq j$, then it is _____ matrix.
   a) Lower triangular b) Upper triangular
   c) Diagonal d) None of these

4) For trapezoidal rule of numerical integration, the Newton-cotes quadrature formula is reduced to _____ points.
   a) 4 b) 2 c) 3 d) 5

5) For initial value problem, the first order ordinary differential equation must be solved for x = _____
   a) x_0 b) x_n c) $x_0 < x < x_n$ d) None of these

6) The empirical relation obtained from least squares fitting for straight line has the form _____

a) $y = ax + b$ b) $y = ax^2 + bx + c$

c) $y = ae^x$ d) $y = \log x$

7) If duty cycle of the function significantly reduces then Fourier spectra changes to _____ spectra.

a) discrete b) continuous

c) monotonic d) all of these

8) If E is the shift operator, then Eyo = _____

a) Y_2 b) Y_3 c) Y_1 d) Y_0

B) State **true** or **false** : **6**

1) The Newton's forward difference formula for 3 points is second order polynomial.

2) Laplace transformation f′ (f) is SF(s) – F(o).

3) Fourier coefficient a_0 for half wave rectifier wave is zero.

4) On Gauss-Jordon elimination, the matrix is reduced to upper triangular matrix.

5) Newton-cotes integration formula for two points reduces to Simpson's $\frac{1}{3}$ rule.

6) Euler's method gives solution of ordinary differential equation.

2. A) Answer **any two** : **10**

1) Write a note on Gaussian elimination.

2) What do you mean by Laplace inverse transformation ?

3) Find Y(15) for following set of points.

x :	0	10	20	30	40
y :	273	283	300	330	340

B) Fit the straight line of the form y = ax + b to the following data : **4**

x :	1	3	5	7	9
y :	1.5	2.8	4.0	4.7	6.0

3. A) What do you mean by system of linear equation ? With suitable example explain Gaussian elimination method for solution of linear equation. **8**

   B) Solve by using Gauss-Jordon method : **6**

   $4x_1 + x_2 - x_3 = -2$

   $5x_1 + x_2 + 2x_3 = 4$

   $6x_1 + x_2 + x_3 = 6$

4. A) What do you mean by interpolation ? With suitable explain Newton's forward difference method for interpolation. **8**

   B) Obtain vapour pressure of water at 27°C using Newton's forward interpolation formula. **6**

f(°C) :	10	20	30	40	50
P(mmtlg) :	9.21	17.54	31.82	55.32	92.51

5. A) Derive Newton-cotes quadrature formula for numerical integration. Describe trapezoidal rule of numerical integration. **8**

   B) Prove that $\frac{\pi}{4} = \int_0^1 \frac{1}{1+x}\,dx$. Use Simpson $\frac{1}{3}$ rule. **6**

6. A) Derive the expression for Fourier coefficient. What do you mean by Dirichlet conditions ? **8**

   B) Find $\frac{dy}{dx}$ at x = 3 for following points. **6**

x :	0	2	4	6	8
y :	0	4	16	36	64

7. A) Define Laplace transform of given function f(t). Prove that $L\,f'(t) = SF(s) - F(o)$. **8**

   B) Describe Langrangian method for unequal interval. **6**

SLR-VS – 10

Seat No.	

M.Sc. – II (Sem. – III) Examination, 2014
ELECTRONICS
Paper – X : Advanced Digital Systems Design with VHDL

Day and Date : Wednesday, 23-4-2014 Total Marks : 100
Time : 3.00 p.m. to 6.00 p.m.

***Instructions** : 1) Answer **five** questions.*
*2) Q. **1** and Q. **2** are **compulsory**.*
*3) Attempt **any three** from Q. **3** to Q. **7**.*
*4) Figures to the **right** indicate **full** marks.*

1. A) Choose correct answer : **8**

1) Every entity has its _____ architecture.
   a) different b) own
   c) mixed d) none of these

2) In case of mixed style of modeling _____ statements are used.
   a) Concurrent assignment b) Process
   c) Component instantiation d) All of these

3) _____ are the EDA tools for front-end design process.
   a) Design entry b) Simulation tools
   c) Synthesis tools d) all of these

4) The _____ statement is used to iterate through a set of sequential statements.
   a) null b) loop
   c) if d) wait

5) Attributes denotes _____ , that characterize various VHDL entity.
   a) types b) functions
   c) value d) all of these

6) The and operator is called _____ operator.
   a) addition b) concatenation
   c) ANDing d) multiplication

7) In VHDL, a bus is a _____ that may have its drivers turned off.
   a) special kind of signal
   b) group of signals
   c) particular method of communication
   d) all of these

8) Generates of an entity are declared along with its ports in _____ declaration.
   a) architecture
   b) entity
   c) process
   d) none of these

B) Fill in the blanks : **6**

1) In package STD-LOGIC – 1164 the meaning of 'X' is _____ (forcing hexadecimal/forcing unknown).
2) Simulation is a _____ way of emulating the behaviour of a circuit. (logical/mathematical)
3) The statement wait for O ns, means to wait for _____ delta cycle. (one/zero)
4) The process statement describes the _____ of an entity. (structure/functionality)
5) The 16 # A # Eg represents _____ ($10 * 16^{9}$ / $10 *^{16} * 9$)
6) A component declaration declares the name and the _____ of a component. (truth table/interface)

C) State **true** or **false** : **6**

1) The process statement is itself a sequential statement.
2) The operators NAND and NOR are not associative.
3) IN : = X "01 – 11 – 00" statement assigns binary value.
4) Test bench is always at the highest level in the hierarchy of the design.
5) The VHDL does not provides the facility to associate user defined attributes with name.
6) The simple Block statement represents only a way of locally partitioning the code.

2. Attempt **any four** : **20**
   1) Explain resolution function.
   2) Explain component declaration with Half Adder.
   3) Explain logical operator.
   4) State the advantages of VHDL.
   5) Explain the block statement.

3. A) Explain in detail basic language elements of VHDL. **10**
   B) Write the VHDL code for 8-bit ALU. **10**

4. A) Explain the architecture with different types. **12**
   B) Write the VHDL code for multiplexer 8 : 1. **8**

5. A) Explain the concurrent statement when and generate. **12**
   B) Write the VHDL code for n × m encoder. **8**

6. A) Discuss process statement in detail with syntax and explain any three process statement. **12**
   B) Write the VHDL code for shift register 4-bit. **8**

7. A) Explain in detail packages and libraries. **12**
   B) Write the VHDL code for 8-bit controlled Inverter. **8**

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SLR-VS – 16

Seat No.	

M.Sc. (Semester – III) Examination, 2014
ELECTRONICS (Elective – 2)
Paper – XII : Computer Aids for VLSI Design

Day and Date : Monday, 28-4-2014 Max. Marks :100
Time : 3.00 p.m. to 6.00 p.m.

Instructions : *1) Answer **five** questions.*
*2) Question **1** and **2** are **compulsory**.*
*3) Attempt **any three** from Q. **3** to Q. **7**.*
*4) Figures to the **right** indicate **full** mark.*

1. A) Choose correct answer : **8**

1) In nMOS environment the metal layer has _____ colour.
a) Green b) Blue c) Yellow d) Red

2) The process of positioning of the cell to establish well connectivity and minimise the space is called
a) Floor planning b) Routing c) Compaction d) All of these

3) The Bus architecture is used to design _____ environment.
a) RTL b) Physical c) Structural d) All of these

4) The prime characteristics of VLSI design is
a) Connectivity b) Hierarchy c) Views d) All of these

5) According to top-to down design flow the last layer of VLSI design is
a) Synthesis b) Analysis
c) Physical d) None of these

6) The FPGA consist of combination of
a) IOB b) CLB
c) Cell d) None of these

7) A cell that does not contain any instances of other cells is at the bottom of the hierarchy is called
a) root cell b) leaf cell
c) composition cell d) none of these

P.T.O.

8) The temporal view design environment uses

a) HDL b) Microwind

c) Xilinix d) None of these

B) Fill in the blanks. **6**

1) In nMOS technology the applied field _____ the flow of current in switched line.

(inhibits, forces).

2) The PLA consists of _____ and _____planes.

(AND-OR, NAND-NOR)

3) Every objects in the VLSI design are associated with _____

(attributes, abstraction)

4) In static analysis _____ is performed.

(GRC, Logical checking)

5) The pictorial representation of 3 domains of VLSI design is

(T chart, Y-chart)

6) The VLSI design is nothing but the aggregation of the _____ in hierarchical manner.

(Cell, Silicon wafer)

C) State **true** or **false**. **6**

1) In temporal simulation the input vectors are in time domain.

2) Behavioural views represents the circuit in description language.

3) The microwind design tool is based on stick diagram.

4) Node extraction is the process of dynamic analysis.

5) The information stored at cell is called as its dimension.

6) The gate matrix consist of columns of the gating element crossing rows of switchable interconnect.

2. Answer **any four** of the following : **20**

   1) Write a note on routing.

   2) What do you mean by electrical rule checking.

   3) Write a note on behavioural level simulation ?

   4) Write a note on branching factor.

   5) Describe Y-chart.

3. a) What do you mean by design characteristics ? Explain in detail the hierarchy. **12**

   b) Describe the architecture of FPGA. **8**

4. a) What do you mean by dynamic analysis ? Explain logic level analysis in detail. **12**

   b) Write a note on programmability. **8**

5. a) What do you mean by representation ? Describe the general issues of representation. **12**

   b) Write a note on stick diagram. **8**

6. a) Describe static analysis in detail. Explain the process of geometrical rule cheking. **12**

   b) Describe the architecture of PLA. **8**

7. a) Describe in detail the VLSI design flow. **12**

   b) Write a note on attributes of an objects. **8**

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Seat No.	

M.Sc. (Part – II) (Semester – IV) Examination, 2014
ELECTRONICS
Paper – XIII : Microwave Devices, Antennas and Measurements

Day and Date : Tuesday, 22-4-2014 Total Marks : 100

Time : 3.00 p.m. to 6.00 p.m.

***Instructions** : 1) Answer **five** questions.*

*2) Questions **1** and **2** are **compulsory**.*

*3) Attempt **any three** from Q. **3** to Q. 7.*

*4) Figures to the **right** indicate **marks**.*

1. a) Choose correct answer : **8**

1) The dominant mode in a rectangular guide with a > b is the _____ mode.

A) TE_{11} B) TE_{10} C) TM_{10} D) TM_{11}

2) Because of its axial symmetry, the conical horn can handle any polarization of the dominant _____ mode.

A) TM_{10} B) TM_{01} C) TE_{11} D) TM_{11}

3) The letter designation 'C band' in commonly used microwave frequency bands indicates the frequency range _____

A) 1 to 2 GHz B) 2 to 4 GHz

C) 4 to 8 GHz D) 26 to 40 GHz

4) An ideal isolator _____

A) is a reciprocal transmission device

B) completely absorbs the power for propagation in one direction

C) provides lossless transmission in the opposite direction

D) both B) and C)

P.T.O.

5) When the standing-wave ratio is _____, there is no reflected wave and the line is called a flat line.

A) 100 B) unity C) infinity D) zero

6) Barretters _____

A) can be made more reproducible in both sensitivity and impedance

B) are less sluggish than thermistors

C) are more sluggish than thermistors

D) both A) and B)

7) 1 watt equals _____ dbm.

A) + 1 B) + 30 C) 0 D) 1000

8) The frequency of oscillation in the LSA mode is _____

A) independent of the transit time of the carriers

B) dependent on the transit time of the carriers

C) Determined solely by the circuit external to the device

D) both A) and C)

b) Fill in the blanks : **6**

1) The _____ horn can give an omnidirectional radiation pattern, and is useful in the VHF-UHF band for broadcasting. (pyramidal/biconical)

2) In n-type GaAs diode the majority carriers are _____ (holes/electrons).

3) An E-plane tee is a waveguide tee in which the axis of its side arm is to the E field of the main guide. (perpendicular/ parallel)

4) In double minimum method of measurement of high VSWR, the shape of the standing wave pattern is observed near voltage _____ (maximum/minimum)

5) For a fixed antenna size, the focusing ability improves as the wavelength _____ (increases/decreases)

6) The distance around the Smith chart once is _____ wavelength. (one-half/one)

c) State **true** or **false** : **6**

1) A basic assumption of ac theory is that the current entering the resistor exactly equals that leaving it, both in amplitude and phase.

2) A transmission line terminated in its characteristic impedance is called a properly terminated line.

3) In Cassegrain antenna the main dish antenna is a hyperboloid while the subdish is paraboloid.

4) The current sensitivity of the detector is defined as the ratio of rectified current to the absorbed r-f power.

5) A matched load termination reflects all the power incident upon it.

6) TEDs are fabricated from compound semiconductors.

2. Write short answers (**any four**) : **20**

a) State and explain Faraday's law of induction.

b) Explain the schematic circuit of a conventional two-conductor transmission line with the distributed constants.

c) What are the fundamental parameters of the bead thermistor ?

d) Explain briefly voltage-controlled and current-controlled modes of negative-resistance devices.

e) Give the schematic diagram of a hybrid ring. What are the characteristics of this device ?

3. a) Discuss the reflection of EM wave from the perfect conductor for normal incidence. **12**

b) What do you mean by VSWR ? **8**

4. a) What are standing waves ? Explain the standing wave patterns in lossy and lossless lines. **12**

b) Give the schematic diagram of a reflex klystron. Explain the process of velocity modulation in this tube. **8**

5. a) Give the schematic diagram of a magic tee. What are the characteristics of this device ? Explain briefly any two applications of this device. **12**

   b) An air filled rectangular waveguide of inside dimensions 1.580 × 0.790 cm operates in the dominant mode. Find

      i) cutoff frequency

      ii) phase velocity of the wave in the guide at a frequency of 14 GHz. **8**

6. a) Give schematic circuit diagram for unbalanced Wheatstone Bridge. Obtain the equation for the bridge sensitivity. **12**

   b) Explain briefly the feed arrangements for microstrip patch antennas. What are the limitations of microstrip antennas ? **8**

7. a) With schematic diagram explain the conventional standing-wave detector method of measurement of VSWR. **12**

   b) With schematic diagram explain the construction of a crystal rectifier. **8**

SLR-VS – 18

Seat No.	

M.Sc. – II (Semester – IV) Examination, 2014
ELECTRONICS
Paper – XIV (Compulsory)
Networking and Data Communication

Day and Date : Thursday, 24-4-2014 Total Marks : 100
Time : 3.00 p.m.to 6.00 p.m.

***Instructions** : 1) Attempt **5** questions.*
*2) Question **1** and **2** are **compulsory.***
*3) Attempt **any three** from Q. **3** to Q. **7**.*
*4) Figures to the **right** indicates **full** marks.*

1. A) Choose the correct alternative : **8**

1) TELNET is general purpose _____ application programme.
   a) Client b) Server
   c) Client/server d) None of these

2) Open Shortest Path First (OSPF) is an implementation of the _____ protocol.
   a) Distance vector b) Link state
   c) Path vector d) All of these

3) The IEEE 802.11 specification covers the _____ layer.
   a) Physical b) Data link
   c) Both a) and b) d) Network

4) The _____ transmission guarantees the frame arrive at a fixed rate.
   a) Synchronous b) Asynchronous
   c) Isochronous d) All of these

P.T.O.

5) In _____ line encoding techniques, the transition at the middle of the bit is used for synchronization.
   a) Manchester and differential Manchester
   b) Manchester
   c) Differential Manchester
   d) None of these

6) Bluetooth uses 2.4 GHz ISM band having _____ channels of _____ bandwidth each.
   a) 79, 1MHz
   b) 79, 4MHz
   c) 256, 1MHz
   d) 256, 4MHz

7) In IPv4 addressing, x. y. z. t/n, in which the n defines the _____
   a) Addresses
   b) Mask
   c) Channels
   d) None of these

8) Routing table may be _____ table.
   a) Dynamic
   b) Static
   c) Dynamic or static
   d) None of these

B) Fill in the blank : **6**

1) RG 58 has a _____ impedance and used for-ethernet. (50, thin/58, thick)

2) IP is an unreliable and connectionless _____ protocol. (Switched/datagram)

3) Several low-rate channels are combined into one high rate channel by using _____ techniques. (TDM/FDM)

4) 48: 01:02:01:26:4B is a _____ address. (Multicast/unicast)

5) In symmetric key cryptography, the key is _____ (Shared/different)

6) A proxy firewall filters at the _____ layer. (Application / network)

C) State **true** or **false** : **6**

1) The bid stuffing is the process of adding one extra 0 whenever five consecutive is follow a 0 in the data.

2) Communication at the network layer in the internet is connection oriented.

3) The 25 channels are used for downstream data and control in ADSL.

4) The effective bandwidth of a digital signal is finite.

5) PPP defines how two devices can authenticate to each other.

6) The network layer is responsible for delivery of datagrams between two host.

2. Answer **any 4** : **20**

1) Explain the transmission impairment.

2) Discuss the frequency hopping spread spectrum.

3) State the deficiencies of IPv4 and advantages of IPv6 over IPv4.

4) Explain QNS in the internet.

5) Discuss SONET network.

3. a) What do you mean by network models ? Discuss the TCP/IP model in detail. **10**

b) Discuss the connecting devices in detail. **10**

4. a) Explain the unicast routing protocol. **10**

b) What do you mean by switched network ? Discuss virtual switched network in detail. **10**

5. a) Explain the IPv4 addressing in detail. **10**

b) Explain ATM. **10**

6. a) Discuss the protocol taxonomy and explain detail HDLC and PPP. **10**

b) What do you mean by QoS ? Discuss techniques to improve QoS. **10**

7. a) What do you mean by standard ethernet ? Explain bridged ethernet. **10**

b) Explain in detail cryptography. **10**

SLR-VS – 19

Seat No.	

M.Sc. (Part – II) (Semester – IV) Examination, 2014
ELECTRONICS
(Paper – XV) : ARM Microcontroller and System Design

Day and Date : Saturday, 26-4-2014 Total Marks : 100

Time : 3.00 p.m. to 6.00 p.m.

***Instructions**: 1) Attempt **five** questions.*
*2) Question **1** and **2** are **compulsory**.*
*3) Attempt **any three** from Q. **3** to Q. **7**.*
*4) Figures to the **right** indicate **full** marks.*

1. A) Select the correct alternatives : **8**

1) AMBA stands for _____.
   a) ARM Microcontroller Bus Architecture
   b) ARM Microprocessor Bus Architecture
   c) Advanced Microcontroller Bus Architecture
   d) None of these

2) ARM7 has _____ stage pipeline.
   a) 3 b) 5 c) 6 d) 7

3) The cache is placed between _____.
   a) Flash memory and registers
   b) Main memory and core
   c) Peripherals
   d) None of these

4) To improve the code density, ARM uses _____.
   a) Thumb 16 bit instruction set
   b) Jazzale 32 bit instruction set
   c) 64 bit instruction set
   d) None of these

P.T.O.

5) ARM core is _____ bit processor.
   a) 8 b) 16 c) 32 d) 64

6) _____ register is the program counter.
   a) r_{15} b) r_{13} c) r_{14} d) r_7

7) When subroutine is called, processor stores return address in _____.
   a) Stack pointer b) Link register
   c) Program counter d) None of these

8) LPC 2378 has _____ flash memory.
   a) 512 KB b) 32 KB c) 8 KB d) 4 KB

B) Fill in the blanks : **6**

1) _____ are unbanked registers.
   ($r_{11} – r_{13}$, $r_0 – r_7$)

2) LPC 2378 has _____ SRAM for Ethernet interface.
   (16 KB, 4 KB)

3) ARM processor can operated in _____ modes.
   (9, 7)

4) ARM processor has a total of _____ registers.
   (37, 32)

5) _____ register is the stack pointer.
   (r_7, r_{13})

6) Jazellel executes _____ bit instructions.
   (8, 16)

C) State **true** or **false** : **6**

1) LPC 2378 has four Timers/counters.

2) ARM supports two types exception.

3) Banked registers r_{13} – SVC, r_{14} – SVC are in undefined mode.

4) Banked register is accessible in all processor modes.

5) When T bit is 0 and J bit is 1, then ARM processor executes Jazellel instruction set.

6) In LPC 2378 ARM 7 TDMI–S processor has two instruction sets.

2. Write short answers **(any four) :** **20**

a) Write a note on current program status register.

b) Mention the salient features of LPC 2378.

c) Describe the pipelining of ARM microcontroller.

d) Write a note on memory organization of LPC 2378.

e) With suitable diagram describe the interfacing of LED to LPC 2378 Microcontroller.

3. a) Explain, with suitable block diagram the architecture of LPC 2378. **12**

b) Write a note on interrupts and Exceptions. **8**

4. a) What do you mean by ARM instruction set architecture ? **12**

b) Write a note on modes of ARM Microcontroller. **8**

5. a) Describe the designing of ARM Microcontroller based an embedded system to measure temperature. **12**

b) What do you mean by barrel shifting ? **8**

6. a) Describe, the ARM core philosophy and AMBA bus architecture in detail. **12**

b) What do you mean by TDMI ? **8**

7. a) Describe register section of the ARM core. Write a note on modes of ARM processor. **12**

b) What do you mean by multiply and accumulate instruction ? **8**

SLR-VS – 2

Seat No.	

M.Sc. (Part – I) (Semester – I) Examination, 2014
ELECTRONICS (CGPA Pattern)
Instrumentation Design (Paper – II)

Day and Date : Wednesday, 23-4-2014 Total Marks : 70
Time : 11.00 a.m.to 2.00 p.m.

***Instructions** : 1) Q. **1** and Q. **2** are **compulsory**.*
*2) Attempt **any three** out of Q. **3** to Q. **7**.*

1. A) Choose correct alternative of the following : **8**

1) LM35 is _____ transducer.
   a) Active b) Passive
   c) Inverse d) None of these

2) The resistance of LDR _____ when exposed to radiant energy.
   a) Remains unaltered b) Increase
   c) Unchange d) Decreases

3) LVDT is an/a _____ transducer.
   a) Magneto-strict ion b) Inductive
   c) Resistive d) Eddy current

4) The following circuit measures and records
   a) A to D convertor b) D to A convertor
   c) Sample and hold d) Data logger

5) LVDT windings are wound on _____
   a) Steel sheets b) Aluminium
   c) Ferrite d) Copper

6) Resolution of transducer depends on _____
   a) Material of wire b) Length of wire
   c) Diameter of wire d) Excitation of wire

7) Self generating type transducers are _____ transducers.
   a) Active b) Passive
   c) Secondary d) Inverse

P.T.O.

8) Pyroelectric sensor is used to measure _____ temperature.

a) Low b) High

c) Both a) and b) d) None of these

B) State **True** or **False** : **6**

1) SAD220 is humidity sensor.
2) Thermocouple is active transducer.
3) Strain gauge is a device that experiences a change in resistance when they are stretched.
4) Optocoupler is used to isolation.
5) AD620 is a programmable instrumentation amplifier.
6) LCD is use to display the parameters measured by instrument.

2. A) Attempt **any two** : **10**

1) Explain 4 to 20 MA current loop.
2) Write note on electro-magnetic relay.
3) Write note on V to I convertor.

B) Explain in detail, isolation amplifier. **4**

3. A) Compare data acquisition and data logger system. **8**

B) Write note on F to V convertor. **6**

4. A) Write note on interfacing of PIR sensor nodules. **10**

B) Compare active and passive sensors. **4**

5. A) Write note on multichannel DAS. **8**

B) Explain signal transmission in detail. **6**

6. A) Write note on signal conditioner (2B30). **8**

B) State static and dynamic characteristics in detail. **6**

7. A) Write note on need of display system in instrumentation. **6**

B) Explain the working of LVDT with the help of diagram. **8**

_____

SLR-VS – 20

Seat No.	

M.Sc. II (Semester – IV) Examination, 2014
ELECTRONICS
Paper – XV : Pro-ASIC System Design

Day and Date : Saturday, 26-4-2014 Max. Marks : 100
Time : 3.00 p.m. to 6.00 p.m.

***Instructions** : 1) Solve **any five** questions.*
*2) Q.**1** and Q.**2** are **compulsory**.*
*3) Solve **any three** from Q.**3** to Q.**7**.*
*4) Figures to the **right** indicate **full** marks.*

1. A) Select correct alternative. **8**

1) The CBIC reduces the risk due to _____ standard cell library.
   a) Preterted b) Predesigned
   c) Precharacterized d) All of these

2) The smallest element of gate array based ASIC is
   a) base cell b) primitive cell
   c) both a & b d) none of these

3) In combinational logic cell an index '1' corresponds to a direct I/P to _____ stage cell.
   a) first b) last c) second d) none of these

4) The metal-metal antifuse link has a resistance of about
   a) 500 $\mu\Omega$ cm b) 500 Ω cm
   c) 500 Ω d) none of these

5) ACT-1 architecture uses _____ antifuse for routing nearby modular.
   a) three b) two c) four d) five

6) The basic cell of Xilinx LCA is an example of a _____ grain architecture.
   a) Coarse b) Fine c) Mixed d) None of these

P.T.O.

7) The programmable ASIC I/O in which _____ connected to bus are called bus transceiver.
   a) input b) output
   c) input & output d) receiver

8) The Elmore delay for each node is
   a) same b) constant c) different d) one

B) Fill in the blanks. **6**

1) ZN = OAI 22 [A, S, B, NOT(S)] is _____ 2 : 1 multiplexer (inverting/ noninverting).

2) The module AVV is a _____ (data path/datapath cell)

3) The clamp diodes in IO cells used to prevent IO pad from voltage excursions _____ than V_{OO} and _____ than V_{SS}. (greater, less/less, greater)

4) All logic cells are predesigned and possibly all mask layers are customized in _____ ASIC. (full custom/semi custom)

5) The capacity of a fixed wiring channel is equal to the number of _____ it contains. (track/hole)

6) The _____ cells for antifuse a programmable low impedance circuit element. (Actel/Xilinx)

C) State **true** or **false**. **6**

1) Antifuse is same of a regular fuse.

2) The flip-flop with a fast clock to QN delay is build using clocked OR gate.

3) Xilinx CLB's contains both combinational logic and flip-flop.

4) The microprocessor is not a ASIC chip.

5) Actel ACT family FPGA the interconnect is fixed at the time of manufacture.

6) The 0.5 μm technology is used for XC 3000 interconnect parameters.

2. Solve **any four**. **20**

1) Explain Elmore's constant.

2) Explain architecture of XC 4000.

3) Write a note on I/O cell.

4) Discuss Shannon's expansion theorem.

5) Explain Gate-array based ASICs.

3. A) What do you mean ACT 1, 2, 3 logic modules ? **12**

   B) Explain pushing bubble concept. **8**

4. A) What do you mean ASIC ? Discuss the different types of ASIC. **12**

   B) Explain RC delays in antifuse. **8**

5. A) Explain in detail different types of parasitic capacitor and issues related to it. **12**

   B) Explain Xilinx programmable IO blocks. **8**

6. A) Explain in detail for ACTEL programmable interconnect. **12**

   B) Explain multiplexer logic as function generator. **8**

7. A) Explain the ACTEL programmable IO cell. **12**

   B) Explain Datapath logic cells. **8**

SLR-VS – 21

Seat No.	

M.Sc. II (Semester – IV) Examination, 2014
ELECTRONICS
Paper – XVI : Industrial Controllers and Automation

Day and Date : Tuesday, 29-4-2014 Total Marks : 100
Time : 3.00 p.m. to 6.00 p.m.

Instructions : *1) Questions No. **1** and **2** are **compulsory**.*
*2) Attempt **any three** questions from question **3** to question **7**.*
*3) Figure to the **right** indicates **full** marks.*

1. A) Choose the correct alternatives : **8**

1) In assembly language, for programming of PLC _____ are used as instruction or function.
a) AND b) OR c) Both a and b c) None of these

2) Z transform of unit impulse function is _____
a) 1 b) 2 c) 3 d) z^{-k}

3) _____ is one of the standard input signal.
a) Ramp b) Voltage c) Current d) All of these

4) CCS is used for _____ control system.
a) Centralize b) Computerize
c) Decentralize d) Both a and b

5) Normally _____ contact, when this contact open, the function carries out some kind of action.
a) Open b) Close
c) Both a and b d) None of these

6) In addition, the coil energization indicates registor _____
a) Negative value b) Positive value
c) Overflow d) All of these

7) ROC of causel system is entire z-plain except _____
a) $|z| = 0$ b) $|z| = \infty$ c) $|z| = -0$ d) $|z| = -\infty$

P.T.O.

8) Normally open and normally close contacts are _____ to each other.
   a) inverse b) proportional
   c) derivative d) none of these

B) Fill in the blanks : **6**

1) On-off controller is _____ controller.
   (linear/non linear)
2) Monitor and _____ the process is one of the feature of DCS.
   (Manuplate/Multiply)
3) CPU is the _____ of the system.
   (Brain/Heart)
4) PLC Registors, input and output are used in bits and also in _____
   (Group/Memory)
5) _____ is standard input signal.
   (Ramp/Error)
6) To program PLC _____ is one of the tool.
   (ladder diagram/C)

C) State whether the following statements are **true** or **false** : **6**

1) Master control relay used for skip next function in PLC programming.
2) CCS stands for centralized computer system.
3) Z transform used in Discrete Control Modeling.
4) Registered input is given to the P/C input directaly.
5) ROC of causel sequence is entire Z-plain except $|z| = 0$.
6) RTU is sensing unit.

2. Attempt **any four** : **20**

1) Write a note on poles and zeros.
2) What do you mean by Networked SCADA system ?
3) What do you mean by Discrete time signal ?
4) Write a note on Z-transform.
5) Write a note on Master Control Relay.

3. A) Explain physical ladder. Give one example for On-off control system and draw PLC ladder architecture for this. **12**

   B) Explain sequencer function with suitable example. **8**

4. A) Describe basic architecture of DCS compare the DCS with CCS. **12**

   B) Write a note on DCS display unit's. **8**

5. A) With suitable diagram explain the architecture of standard PLC. **12**

   B) Explain simple second order system. **8**

6. A) With suitable Block diagram. Explain architecture of control system. **12**

   B) Explain transformation of z to w domain. **8**

7. A) Explain the term Industrial Automation. Describe in detail, basic architecture of DCS. **12**

   B) What do you mean by poles and zeros ? **8**

SLR-VS – 22

Seat No.	

M.Sc. – II (Semester – IV) Examination, 2014
ELECTRONICS
Paper – XVI : Wireless Sensor Network

Day and Date : Tuesday, 29-4-2014 Total Marks : 100

Time : 3.00 p.m. to 6.00 p.m.

***Instructions**: 1) Attempt **5** questions.*
*2) Questions **1** and **2** are **compulsory**.*
*3) Attempt **any three** from **Q. 3** to **Q. 7**.*
*4) Figures to **right** indicate **full** marks.*

1. A) Choose correct alternatives : **8**

1) The primary component of WSN is
   A) Sensor B) Mobile station
   C) Base station D) Access point

2) IEEE 802.11 and 802.11 b operate at
   A) 1.4GHz B) 2.4GHz
   C) 3.4GHz D) 5GHz

3) WPAN formed under _____ standard.
   A) IEEE 802.11 B) IEEE 802.15
   C) IEEE 802.16 D) IEEE 802.20

4) The basic fixed assignment multiple access method are
   A) FDMA B) TDMA C) CDMA D) all

5) _____ protocol stand for bluetooth.
   A) IEEE 802.15.1 B) IEEE 802.15.3
   C) IEEE 802.15.4 D) IEEE 802.15.6

6) X.25 provide standard connectionless network access protocol for _____ layer of OSI model.
   A) Lowest three B) Upper three
   C) Lowest four D) Upper four

7) Mobile Ad-Hoc network also called as _____.
   A) Mobile bus network B) Mobile ring network
   C) Mobile mesh network D) Mobile hybrid network

8) Packet reservation multiple access (PRAM) is _____ protocol.
   A) Receiving B) Transmission
   C) Both A & B D) None of these

B) Fill in the blanks : **6**

1) IEEE standard for zigbee is _____.
   (802.15.1, 802.15.4)
2) Interest describe _____.
   (Task required to be done, direction)
3) Energy dissipation is _____ in flat top routing.
   (uniform, non-uniform)
4) Lower energy node in Hierarchical type of routing used to _____.
   (Sensing, Processing)
5) CDMA system are implemented based on the _____ technique.
   (Spread spectrum, relay)
6) MAC stand for _____.
   (Media Access Control, Mobile Access Control)

C) State **True** or **False** : **6**

1) Base Station Subsystem (BSS) also known as radio sub system.
2) Hierarchical routing requires only global synchronization.
3) IN flat top routing all node play different role.
4) LEACH is cluster based protocol.
5) GSN stand for globally support node.
6) Wireless Ad-Hoc sensor network are infrastructure wireless network.

2. Attempt **any four** : **20**

   1) Explain MAC management syblayer in 802.11 wireless LAN.

   2) Explain three tiered architecture of sensor network.

   3) Write a note on cluster gateway switch routing protocol.

   4) Give difference between wired and wireless network.

   5) Write a note on CDMA.

3. a) Explain 802.15 wireless networking protocol. **14**

   b) Explain physical layer in 802.11. **6**

4. a) Explain power efficient topologies for wireless sensor network. **10**

   b) Give taxonomy of routing technique in wireless network. **10**

5. a) Draw and explain modeling of dynamic wireless network. **12**

   b) Draw and explain layered structure of GPRS. **8**

6. a) What is the need of energy management ? Explain battery management scheme and system power management scheme. **12**

   b) Write a note on : **8**

      1) Integrity

      2) Authentication

      3) Localization

      4) Attack mechanism.

7. a) Explain zigbee the RF module. **12**

   b) Give the specification of WSN devices and on chip resources of zigbee module. **8**

SLR-VS – 23

Seat No.	

M.Sc. (Part – II) (Semester – IV) Examination, 2014
ELECTRONICS
Paper – XVI : Mixed Signal Soc Design

Day and Date : Tuesday, 29-4-2014 Total Marks : 100
Time : 3.00 p.m. to 6.00 p.m.

Instructions : *1) Attempt **five** questions.*
*2) Questions **1** and **2** are **compulsory**.*
*3) Attempt **any three** from Q. **3** to Q. **7**.*
*4) Figures to the **right** indicate **full** marks.*

1. A) Select correct alternatives : **8**

1) In case of cypress PSOC1 the digital blocks are arranged in array of
a) Rows b) Columns c) 8 bytes d) 16 bytes

2) The PSOC⊥ device comprise the _____ pages in the SRAM.
a) 2 b) 4 c) 3 d) none of these

3) The cypress PSOC5 consists of the microcontroller core of _____ operating at back end.
a) M8C b) AVR c) ARM d) PIC

4) In $(D - \Sigma)$ delta-sigma ADC the sampling frequency configured is
a) $f_S <= f_N$ b) $f_S = f_N$
c) $f > f_N$ d) None of these

5) In switched capacitor block two clock pulses should satisfy the relation
a) ϕ_1 and ϕ_2 should in phase b) ϕ_1 and ϕ_2 should out of phase
c) $\phi_1 = \phi_2$ d) None of these

6) In continuous time analog block _____ analog input can be configured.
a) 2 b) 4 c) 3 d) 5

P.T.O.

7) In high precision clock mode to obtain the clock of 24 MHz _____ divisor is used in PLL block.

a) 732 b) 16 c) 256 d) 512

8) The essential stage of CMOS operational amplifier is

a) Buffer b) Feed back

c) Current mirror d) None of these

B) Fill in the blanks : **6**

1) The M8C microcontroller has the register banks of _____ bytes [16, 256].

2) The quantizer used in delta sigma ADC decides _____ [resolution, frequency]

3) The sinking current capacity of PSOC device is _____ [10 mA, 25 mA]

4) The programmable timer block has _____ bit max. resolution. [8, 24]

5) _____ bit of status register must be set for interrupt enable [IE, GIE]

6) In switch capacitor block _____ is configured by switch capacitor principle. [Inductor, Resistor]

C) State **true** or **false** : **6**

1) The clock source Vc_2 is obtained from Vc_1.

2) PSOC devices does not consist the microcontroller.

3) Analog building block in PSOC device is not programmable.

4) The M8C microcontroller consist of only one ADC.

5) The input impedance of BiCMOS is very high.

6) In CMOS transistor, the P well indicates less amount of P concentration.

2. Attempt **any four** of the following : **20**

1) Write a note on the term reconfiguration.

2) Describe the system bus architecture of PSOC1.

3) Differentiate the concept of system-on-Board and system-on-chip.

4) Write a note on programmable gain amplifier.

5) Write a note on first order delta sigma modulation ADC.

3. A) Discuss the principle of switched capacitor. Describe switched capacitor analog block of PSOC device. **12**

   B) Write a note on CMOS transistor. **8**

4. A) What do you mean by mixed signal technology ? Describe the system clock of PSOC device. **12**

   B) Write a note on I/O ports of PSOC. **8**

5. A) Describe in detail the programmable digital block of PSOC. **12**

   B) Describe the architecture of M8C controller. **8**

6. A) Describe, with suitable block diagram the delta-sigma ADC of PSOC. **12**

   B) What do you mean by clock Jitter and its impact on ADC performance ? **8**

7. A) Describe in detail the designing SOC for humidity measurement. **12**

   B) Write a note on Touch sensing. **8**

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SLR- VS – 3

Seat No.	

M.Sc. – I (Semester – I) Examination, 2014
ELECTRONICS (CGPA Pattern)
Paper – III : Power Electronics

Day and Date : Friday, 25-4-2014 Max. Marks : 70
Time : 11.00 a.m. to 2.00 p.m.

Instructions *: 1) Q. **1** and Q. **2** are **compulsory**.*
*2) Solve **any three** from Q. **3** to Q. **7**.*
*3) Figures to the **right** indicate **full** marks.*

1. A) Choose correct alternative : **8**

1) In unidirectional AC voltage controller, the power flow is controlled by during _____

a) +ve half cycle b) –ve half cycle
c) +ve and –ve half cycle d) All of these

2) In a dual converter one and two work in _____

a) Rectifying and inversion b) Both in rectifying
c) Both in inversion d) None of these

3) Output voltage of step-up chopper is given by _____ relation.

a) $V_s (1 – K)$ b) $V_s / (1 – K)$
c) KV_s d) None of these

4) The number of thyristors required for single phase cycloconverter of mid-point type and for three phase to three phase there pulse type cycloconverter are respectively _____

a) 4, 6 b) 4, 18
c) 8, 18 d) 4, 36

5) Output voltage of a single phase bridge inverter feed from fixed DC source is varied by _____

a) PWM
b) PAM
c) Varying the switching frequency
d) All of above

P.T.O.

6) Simplest method of eliminating 3rd harmonics from the output voltage waveform of single phase bridge inverter is to use _____

a) Single pulse modulation b) Multiple pulse modulation

c) Inverter in series d) Stepped wave inverter

7) A chopper in which current remains +ve but voltage may be +ve or –ve is known as _____

a) Type A b) Type B

c) Type C d) Type D

8) In DC chopper if T-ON is the ON period and F is the chopping frequency then output voltage in terms of input voltage Vs is given by _____

a) Vs TON/F b) Vs F/TON

c) Vs/F-TON d) Vs.F.TON

B) State **true** or **false** : **6**

1) Semiconverter is two quadrant converter.

2) A free-wheeling diode is also called as commutating diode.

3) In controlled rectifier the input voltage is controlled by controlling the firing angle of thyristors.

4) Cycloconverter is a AC to AC converter.

5) For $\alpha > 90°$ the three phase full converter operator in rectification mode.

6) The flow of power in the circuit is always from AC side.

2. A) Solve **any two** : **10**

1) Discuss advantages and disadvantages of controlled rectifier.

2) Discuss the effect of only cycle on phase control.

3) Explain PWM inverter.

B) Explain need of free wheeling diode. **4**

3. A) Explain the principle of step-up chopper with resistive load and derive necessary equations. **8**

   B) Write note on chopper controlled strategies. **6**

4. A) Explain single phase AC bidirectional voltage controller with resistive load and derive the output relation. **8**

   B) Explain principle of ON-OFF controller in detail. **6**

5. A) Explain three phase half wave controlled rectifier and derive output equations. **8**

   B) Write a note on three phase full wave full controlled bridge rectifier with resistive load. **6**

6. A) What is principle of cycloconverter ? Explain single phase cycloconverter in detail. **8**

   B) Explain operation of single phase bridge inverter. **6**

7. A) Draw the circuit of dual converter and explain its working using waveforms. **8**

   B) What is mean by power factor improvement. **6**

SLR-VS – 4

Seat No.	

M.Sc. (Part – I) (Semester – I) Examination, 2014
ELECTRONICS (CGPA Pattern)
Paper – IV : Advanced Microcontrollers

Day and Date : Monday, 28-4-2014 Total Marks : 70

Time : 11.00 a.m. to 2.00 p.m.

***Instructions**: 1) Answer **any five** questions.*

*2) Questions **1** and **2** are **compulsory**.*

*3) Attempt **any three** from Q. **3** to Q. **7**.*

*4) Figures to the **right** indicate **full** marks.*

1. a) Choose correct answer : **8**

1) The program memory capacity of PIC 16F877 is

A) 1KB B) 8KB C) 14KB D) 32KB

2) There are _____ single word instructions in PIC 16F877.

A) 25 B) 35 C) 72 D) 104

3) PIC 16F877 has _____ pins.

A) 16 B) 32 C) 40 D) 64

4) The general purpose registers in ATMega 8 are

A) 16 B) 32 C) 8 D) 4

5) The on-chip RAM memory capacity in ATMega 8 is

A) 512 Bytes B) 512 KB C) 512 MB D) None of these

6) _____ are available on-chip in AVR.

A) RAM and ROM B) Timers and counters

C) ADC D) All of these

7) LCD module have _____ pin for selection of registers.

A) RS B) $\overline{EN}$ C) $\overline{CS}$ D) R/W

8) PWM output can be achieved by using

A) Delay routine B) Timers C) Counters D) All of these

P.T.O.

1. b) State **true** or **false** : **6**

   1) Micro C can be used for development of programs for embedded systems.
   2) Memory interfacing can be achieved using I/O mapped I/O method.
   3) OLED consumes more power as compare to LED.
   4) Matrix type keyboards reduces the I/O line requirement.
   5) AVR has on-chip RAM and ROM.
   6) PIC microcontrollers have built in EPROM.

2. A) Attempt **two** : **10**

   a) Enlist the features of AVR series microcontrollers.
   b) State the advantages of PIC over MCS-51 microcontrollers.
   c) Explain the need of interfacing of I/O devices.

   B) Explain the utilities of timers and counters in microcontroller. **4**

3. a) Explain general architecture of AVR microcontroller. **8**

   b) Explain configuration of ADC with PIC. **6**

4. a) Explain development of embedded system for temperature control using PIC. **8**

   b) What are the advantages of bit oriented instructions ? Explain any five bit oriented instructions of PIC16F877. **6**

5. a) What do you mean by PWM ? Explain how it can be used to control the speed of DC motor. **8**

   b) Explain the procedure of developing project using MPLAB. **6**

6. a) Explain arithmetic instructions of AVR microcontroller with the help of examples. **8**

   b) Explain interfacing of matrix type key board with AVR. **6**

7. a) Explain conditional branching instructions of AVR with examples. **8**

   b) Explain the procedure for development of application using AVR microcontroller with the help of any one integrated development tool. **6**

SLR-VS – 5

Seat No.	

M.Sc. (Part – I) (Semester – II) Examination, 2014
ELECTRONICS (New) (C.G.P.A. Pattern)
Paper – V : Control Theory

Day and Date : Tuesday, 22-4-2014 Total Marks : 70
Time : 11.00 a.m. to 2.00 p.m.

***Instructions** : 1) Answer **five** questions.*
*2) Question **1** and **2** are **compulsory**.*
*3) Attempt **any three** from Q. **3** to Q. **7**.*
*4) Figures to the **right** indicates **full** marks.*

1. A) Choose correct answer : **8**

1) _____ time is the time required for the response to reach 50% of the final value in the first attempt.
a) Delay b) Rise c) Peak d) Settling

2) A signal flow graph is a graphical representation of relationship between the variables of _____ algebraic equation.
a) Linear b) Non-linear c) Exponential d) None of these

3) In second order control system breaks into continuous oscillations for _____
a) $\xi < 1$ b) $\xi > 1$ c) $\xi = 1$ d) $\xi = 0$

4) If all roots of the characteristics equation have _____ parts then the system is stable.
a) Negative real b) Positive real
c) Negative imaginary d) Positive imaginary

5) Laplace transform of unit impulse is _____
a) 1/s b) 0 c) 1 d) ∞

6) In force voltage analogy of the system force is equivalent to _____
a) Voltage b) Current c) Inductance d) Capacitance

7) In the system if the poles lie of the real axis, then the system is _____
a) Over damped b) Critical damped
c) Under damped d) None of these

8) In a signal flow graph a dummy branch has a gain of _____
a) Unity b) Infinity c) Constant d) None of these

P.T.O.

B) State **True** or **False** : **6**

1) Open control system does not possess self correcting ability.
2) Root locus is symmetrical above the real and imaginary axis.
3) Back emf in DC shunt motor is directly dependent on speed.
4) Loop is a path which originates and terminates at the same node.
5) Bode plot is convention of multiplicative factor into additive factor.
6) The corner frequency divide only low frequency region.

2. A) Attempt **two** (short questions) : **10**

a) What is transfer function ? Write its advantages and disadvantages.
b) Compare open loop and closed loop system.
c) Write a note on polar plot.

B) Rules for block diagram reduction technique. **4**

3. A) Characteristics equation of a feedback system is $F(s) = S^4 + 2S^2 + 1$ using routs criteria determine stability of the system. **8**

B) Explain concept of poles and zeros. **6**

4. A) Explain the procedure for obtaining bode plot for $G(j\omega)$ express in time constant form. **8**

B) Explain root locus technique. **6**

5. A) Explain proportional plus integral action. **8**

B) Discuss the time response of first order system. **6**

6. A) How feedback control systems are classified as type-I and type-II ? **8**

B) Explain the need of standard test signal. **6**

7. A) Explain the concept and construction of root locus for second order system. **8**

B) Explain the term dead time and control lag. **6**

SLR-VS – 6

Seat No.	

M.Sc. (Part – I) (Semester – II) Examination, 2014
ELECTRONICS (New)
(C.G.P.A. Pattern)
Paper – VI : Real Time Operating System

Day and Date : Thursday, 24-4-2014 Total Marks : 70

Time : 11.00 a.m. to 2.00 p.m.

Instructions *: 1) Attempt* ***five*** *questions.*
2) Question No. 1 and ***2*** *are* ***compulsory****.*
3) Answer ***any three*** *from Q.* ***3*** *to Q.* ***7****.*
4) Figures to the ***right*** *indicate* ***full*** *marks.*

1. A) Select correct alternatives : **8**

1) For small scale embedded system _____ is optional.

a) Operating system b) Super loop

c) Micro controller d) None of these

2) A task of O priority is called _____ task.

a) System b) Ideal

c) Idle d) Main

3) _____ following is good humidity sensor.

a) TGS 4161 b) LM 375

c) MQ 7 d) SY-HS-220

4) On release, the mutex counter _____

a) Decrements b) Increments

c) Remains unchanged d) None of these

5) _____ is the solution to avoid dead lock.

a) Priority b) Semaphore

c) Queue d) Context switching

P.T.O.

6) On of _____ into Linux Kernel the RT Linux Kernel is formed.

a) Scheduler b) Memory Management

c) Real time Kernel d) ISR

7) In priority based pre-emptive scheduling mechanism _____ task would be pre-emptited.

a) Higher priority b) Lowest priority

c) Idle task d) None of thee

8) The function _____ is used in RT Linux programming to stop the execution of thread.

a) Pthread – int – module ( ) b) Cleanup – module ( )

c) Pthread – stop – module ( ) d) None of these

B) State **true** or **false** : **6**

1) Dynamic priority solves the problem of priority inversion.

2) On collapsing of dead line the hard real time operating system results in catastrophic change.

3) The Micro C/OS-II Kernel is based on Rate monotonic scheduling mechanism.

4) For an embedded system either hardware or software is essential.

5) To ensure intertask communication message box is enabled.

6) Each task should associate with the priority and stack size.

2. A) Attempt **any two** : **10**

1) Give salient features of an embedded system.

2) Write a note of structure of the task.

3) What are advantage of Micro C/OS-II Kernel ?

B) What do you mean by intertask communication ? **4**

3. A) Describe minimum requirement of micro controller based on embedded system. **8**

   B) Design an embedded system to measure temperature of heater. **6**

4. A) What do you mean by resource synchronization for tasks ? Explain the use of semaphore to avoid the dead lock. **8**

   B) Describe Priority inversion mechanism. **6**

5. A) Define the term scheduling ? Describe with suitable diagram priority-based pre-emptive scheduling. **8**

   B) Write a note on context switching. **6**

6. A) Describe in detail the architecture of RTOS. Explain the types of real time embedded system. **8**

   B) Describe in details the task states machine. **6**

7. A) Describe the architecture of RT Linux Kernel. **8**

   B) Write a short note creation of task in Micro C/OS-II Kernel. **6**

SLR-VS – 7

Seat No.	

M.Sc. (Part – I) (Semester – II) Examination, 2014
ELECTRONICS (New) (CGPA Pattern)
Paper – VII : Opto Electronics

Day and Date : Saturday, 26-4-2014 Total Marks : 70

Time : 11.00 a.m. to 2.00 p.m.

***Instructions**: 1) Q. **1** and Q. **2** are **compulsory**.*

*2) Solve **any three** from Q. **3** to Q. **7**.*

*3) Figures to the **right** indicate **full** marks.*

*4) **All** questions carry **equal** marks.*

*5) Answer **five** questions.*

1. A) Choose correct alternative : **8**

1) _____ optical fibers do not have constant refractive index in the core.

a) Step index b) Graded c) Both a & b d) None of these

2) Numerical aperture is the measure of _____ efficiency of the fiber.

a) Light gathering b) Light rejection

c) Light dispersion d) None of these

3) A wavelength of light emitted by the material of band gap E_g is given by λ = _____

a) $\frac{1}{E_g}$ b) $\frac{1.24}{E_g}$ c) $\frac{0.6}{E_g}$ d) $\frac{0.3}{E_g}$

4) In case of Laser diode, the phenomenon of _____ is taking place.

a) Population inversion b) Absorption

c) Amplification d) None of these

P.T.O.

5) The photo diodes are always in _____ bias mode.
   a) forward b) reverse
   c) unbiased d) none of these

6) In semiconductor photo detectors, the charge carrier pairs, due to photons of light are formed at _____ region.
   a) P b) N
   c) depletion layer d) none of these

7) _____ is the phenomenon in which the incident light beam is doubly refracted.
   a) Refraction b) Birefringance
   c) Optical activity d) None of these

8) For half wave retarding plate the phase difference between O and E waves is _____
   a) 90° b) 180° c) 120° d) 360°

B) State **true** or **false** : **6**

1) Optical devices are based on the principle of indirect semiconducters.

2) If the refractive index of the material varies as a function of wavelength of light then pulse amplitude modulation takes place.

3) He-Ne is good source for optical communication.

4) Splicing is the method of joining of the optical fibers.

5) Optically isotropic crystals do not used for light modulation.

6) In AO effect the refractive index of the material varies with piezoelectric strain.

2. A) Solve **any two** from the following : **10**

1) Describe the phenomenon of total internal reflection.

2) Describe the method of fiber loss measurement.

3) Write a note on PIN diode.

B) What do you mean by polarization ? Describe birefringance phenomenon. **4**

3. A) With working principle, describe the use of photodiode as optical detectors. **8**

   B) What do you mean by step and graded index fiber ? **6**

4. A) Describe He-Ne Laser source with its spectral and spatial characteristics. **8**

   B) Describe working principle of avalanche diode. **6**

5. A) What do you mean by phase modulation ? Describe Pockel effect and discuss use of pockel cell as modulator. **8**

   B) What do you mean by intensity modulation ? Describe Pockels intensity modulator. **6**

6. A) With basic principle describe Acoustic Optic (AO) effect for intensity modulation. **8**

   B) Write a note on magneto optic devices. **6**

7. A) Describe the methods of optical fiber fabricaiton. **8**

   B) Describe the terms half wave plates and quarter waveplates. **6**

SLR-VS – 8

Seat No.	

M.Sc. (Part – I) (Semester – II) Examination, 2014
ELECTRONICS (New) (CGPA Pattern)
Paper – VIII : Electronic Circuit Design

Day and Date : Tuesday, 29-4-2014 Total Marks : 70

Time : 11.00 a.m. to 2.00 p.m.

Instructions *: 1) Answer **five** questions.*
*2) Question **1** and **2** are **compulsory**.*
*3) Attempt **any three** from Q. **3** to Q. **7**.*
*4) Figures to the **right** indicates **full** marks.*

1. a) Choose correct answer. **8**

1) A-bit ripple counter consists of flip-flop that each have a propagation delay from clock to Q output of 12 ns. For the counter to recycle from 1111 to 0000, it takes a total of

a) 12 ns b) 24 ns c) 48 nc d) 144 ns

2) The output capacitance of 78XX regulator remover the _____ in the voltage regulator.

a) Effect of story inductance b) Transient response

c) Ripple d) None of these

3) In the phase shift oscillator frequency of oscillation F0 is

a) $\frac{1}{2\pi RC\sqrt{6}}$ b) $\frac{1}{2\pi RC}$ c) $\frac{1}{2\pi\sqrt{RC}}$ d) 0.693 RC

4) CMOS schmitt triggers offers the advantage of high _____ and low _____ consumption.

a) input impedance, power b) output impedance, power

c) input impedance, energy d) output impedance CMRR

5) The quiescent current IQ in the 78XX series is

a) 4 mA b) 4.2 mA c) 4.2 μ A d) 4.2 A

P.T.O.

6) The Ton for astable multivibrator is

a) $0.693\ (R_A + R_B).C$ b) $0.693(2R_A + R_B)C$

c) $0.693\ R_A.C$ d) $0.693\ R_B.C$

7) The equation in lock in range is

a) $\Delta f_L = \pm \frac{7.8 f_O}{V}$ b) $\pm \sqrt{f_l \Delta f_i}$ c) $f_O + K_V.V_C$ d) $\Delta f = f_s - f_o$

8) A-4-bit binary counter has a maximum modulus of

a) 16 b) 32 c) 64 d) 4

b) State **true** or **false**. **6**

1) Rom are commonly available in size from 256 to 65,536 bits with 4 or 8 output lines.

2) 74121 is triggerable monostable multivibrator.

3) A triangular wave can simply obtained by integrating a square wave.

4) An example of synchronous decade counter is 7490.

5) Typical value of line regulation from the data sheet of 7805 is 3mV.

6) CD 7414 is CMOS inverting schmitt trigger.

2. A) Attempt **any two**. **10**

1) Write a note on PID controller.

2) Explain monostable multivibrator using gate.

3) Write a note on memory interfacing.

B) Convert 101011100 binary code to gray code using Exor gate. **4**

3. a) State the advantages of IC voltage regulator over discrete voltage regulator. Explain in brief 78XX series IC regulator. **8**

b) Write a note on series voltage regulator. **6**

4. a) Design a timer circuit to control the heater from time duration 1 sec to 100 sec using relay of 12 V/150 mA. **8**

   b) Design RC phase shift oscillator using op-amp for frequency of 900 KHz. **6**

5. a) Explain in detail triangular wave generator and derive the frequency relation. **8**

   b) Write a note on CMOS to TTL interface. **6**

6. a) Explain a need of parity bit. Design a parity checker. **8**

   b) How design a digital multimeter ? **6**

7. a) Explain in detail PLL and derive the relation for capture in range. **8**

   b) Design mod 7-synchronous counter using JK flipflop. **6**

SLR-VS – 9

Seat No.	

M.Sc. (Part – II) (Semester – III) Examination, 2014
ELECTRONICS
Digital Signal Processing (Paper – IX)

Day and Date : Monday, 21-4-2014 Total Marks : 100
Time : 3.00 p.m. to 6.00 p.m.

Instructions *: 1) Answer* ***five*** *questions.*
2) Question ***1*** *and* ***2 compulsory****.*
3) Attempt ***any three*** *from Q.* ***3*** *to Q.* ***7****.*

1. A) Choose the correct answer : **8**

1) The ROC statement for causal sequence is _____
   a) Entire z-plane except | z | = ∞
   b) Entire z-plane except | z | = 0
   c) Entire z-plane except | z | = 0 and |z| = ∞
   d) None of these

2) In discrete time signal the condition of periodicity is _____
   a) x(n) = x(n + N) b) x(t) = x(t + T_0)
   c) x(n) = x(n – N) d) x(t) = x(t – T_0)

3) _____ system do not require any past output sample to calculate the present output.
   a) Recursive b) Non-recursive
   c) Causal d) Static

4) The region of convergence of the z-transform of unit step function is
   a) | z | > 1 b) | z | < 1
   c) Real part of z > 0 d) Real part of z < 0

5) Signum function is represented as
   a) $\text{sgn}(t) = \begin{cases} 1 & \text{for } t < 0 \\ -1 & \text{for } t > 0 \end{cases}$ b) $\text{sgn}(t) = \begin{cases} 1 & \text{for } t > 0 \\ -1 & \text{for } t < 0 \end{cases}$
   c) sgn(t) = 1 d) sgn(t) = x(2n)

P.T.O.

6) Fourier transform exist only if _____ signal is absolutely summable.
   a) Discrete time b) Continuous time
   c) Both a) and b) d) None of these

7) Auto-correlation is denoted by _____
   a) $r_{xx}(l)$ b) $r_{xy}(l)$ c) $r_x(l)$ d) $r_y(l)$

8) Which of the following represents the z-transform of unit ramp function ?
   a) $\frac{z}{(z-1)^2}$ b) $\frac{z}{z-1}$ c) $\frac{1}{(z-1)^2}$ d) $n \cdot u(n)$

B) Fill in the blanks : **6**

1) $x_N = \frac{1}{N}[W_N^*]X_N$, in given function '$*$' indicates _____
   (Convolution, Complex-conjugate)

2) A relaxed system means if input x(n) is zero, then output y(n) is _____
   (zero, finite)

3) Attenuation means _____ the amplitude of signal.
   (increasing, reducing)

4) If x(t) = –x(–t) the signal is said to be an _____ signal.
   (odd, even)

5) Dynamic system are with _____
   (memoryless, memory)

6) X(w) is periodic because discrete time signals are having limited range _____
   (o to 2π, $-\pi$ to $\frac{\pi}{2}$)

C) State **true** or **false** : **6**

1) $y(n) = x^2(n) + 5x(n) + 10$ is a static system.

2) The zeros of z-transform are the values of z for which $X[z] = \infty$.

3) Ideal filters are practically not realizable.

4) Triangular window produces smoother magnitude response than that of rectangular window function.

5) LTI system is stable if its impulse response is absolutely summable.

6) Folding and time delaying or advancing of a signal are commutative.

2. Attempt **any four** : **20**

   1) Differentiate between z-transform and DFT.

   2) Explain standard test signal.

   3) Compute $y(n) = x(n) * h(n)$, if $x(n) = h(n) = \{1, 2, -1, 3\}$.

   4) Z-transform of unit step signal.

   5) Explain non-recursive system.

3. a) How LTI system is stable if its impulse response is absolutely summable ? **10**

   b) Determine whether the following system are linear or not : **10**

      i) $y(n) = x(n^2)$

      ii) $x(n) + nx(n + 1) = y(n)$.

4. a) What is z-transform ? Obtain the z-transform and ROC of finite duration signal.

   $x(n) = \{2, 4, \underset{\uparrow}{5}, 7, 0, 1\}$ **10**

   b) State and explain any four properties of z-transform. **10**

5. a) Determine the 8-point DFT of the sequence $x(n) = \{1, 2, 1, 2\}$. **10**

   b) Why the result of circular and linear convolution is not same ? How to obtain same result ? **10**

6. a) State and prove differentiation and convolution theorem of FT. **10**

   b) Obtain Fourier transform of single sided exponential pulse. **10**

7. a) Determine the parallel realization of the IIR digital filter transfer function.

   $$H(z) = \frac{1 + 2z^{-1} + z^{-2}}{1 - 0.75z^{-1} + 0.125z^{-2}} .$$ **10**

   b) Explain the procedure for designing an FIR filter using window method. **10**
